What is claimed:

1. A method of forming a metal wiring in a semiconductor device, the method comprising:

providing a substrate with a lower metal layer overlying the substrate and an interlayer insulating film comprising first, second and third insulating films formed on the lower metal layer;

forming a damascene pattern comprising a trench and a via on the interlayer insulating film, a portion of the second insulating film forming a bottom of the trench, a portion of the lower metal layer forming a bottom of the via, the trench and the via each comprising a sidewall;

forming diffusion prevention film spacers on the sidewalls of the trench and the via;

selectively forming chemical enhancer layers on the portion of the second insulating film forming the bottom of the trench and on the portion of the lower metal layer forming the bottom of the via;

forming a copper layer on the diffusion prevention film spacer and chemical enhancer layers by means of chemical vapor deposition method; and

performing a hydrogen reduction annealing and a chemical mechanical polishing process to form a copper metal wiring from the copper layer.

2. The method of claim 1, wherein the lower metal layer is W or Al and the method further comprises a cleaning process performed after formation of the damascene pattern, the cleaning process comprising exposing the lower metal layer to a RF plasma.

3. The method of claim 1, wherein the lower metal layer is made of Cu, and the method further comprising a cleaning process performed after formation of the damascene pattern, the cleaning process comprising exposing the lower metal layer to a reactive cleaning.

4. The method of claim 1, wherein the diffusion prevention spacer is formed by forming a diffusion film having a thickness ranging from about 50 to about 500 Å on the entire structure including the damascene pattern and then performing a blanket etch process.

5. The method of claim 1, wherein the diffusion prevention film spacer comprises at least on material selected from the group consisting of ionized PVD TiN, CVD TiN, MOCVD TiN, ionized PVD Ta, ionized PVD TaN, CVD Ta, CVD TaN, CVD WN, CVD TiAlN, CVD TiSiN and CVD TaSiN.

6. The method of claim 1, wherein the diffusion prevention film spacer is formed by using SiN or SiON.

7. The method of claim 1, wherein the chemical enhancer layers are formed in a thickness ranging from about 50 to about 500 Å, using a catalyst, selected from the group consisting of I (iodine)-containing liquid compound, Hhfac1/2H_2O, Hhfac, TMVS, pure I_2, I (iodine)-containing gas, and water vapor at a temperature ranging from about -20 to about 300°C for a time period ranging from about 1 to about 600 seconds.

8. The method of claim 7, wherein the catalyst is an I (iodine)-containing liquid compound selected from the group consisting of CH_3I, C_2H_5I, CD_3I and CH_2I_2.

9. The method of claim 1, wherein the chemical enhancer layers are formed in a thickness ranging from about 50 to about 500Å, using a catalyst selected from the group consisting of F, Cl, Br, I and At in a liquid state at a temperature ranging from about -20 to about 300°C for a time period ranging from about 1 to about 600 seconds.

10. The method of claim 1, wherein the chemical enhancer layers are formed in a thickness ranging from about 50 to about 500Å, using a catalyst selected from the group consisting of F, Cl, Br, I and At in a gas state at a temperature ranging from about -20 to about 300°C for a time period ranging from about 1 to about 600 seconds.

11. The method of claim 1, wherein the copper layer is formed in a deposition apparatus by means of metal organic chemical vapor deposition (MOCVD) method, by using one or more precursors selected from the group consisting of hfac such as (hfac)CuVTMOS series, (hfac)CuDMB series, and (hfac)CuTMVS series.